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IT IS CLAIMED:

1. In a non-volatile memory including an array of charge storage elements positioned over a substrate surface between source and drain regions, a method of altering or determining charge states of designated ones of the storage elements, comprising:

applying first voltage levels to at least a first and a second control gates that are both capacitively coupled with the designated storage elements to combine to cause the charge states of the designated storage elements to be either altered or determined,

simultaneously applying a second voltage level to at least a third control gate that is capacitively coupled with a first group of non-designated storage elements that are also coupled with one of the first or second control gates to combine to cause the charge states of the first group of non-designated storage elements to be neither altered nor determined, and

simultaneously applying third voltage levels to additional control gates to which other non-designated storage elements are capacitively coupled with at least two thereof to combine to cause the charge states of the other non-designated storage elements to be neither altered nor determined.

2. The method of claim 1, wherein the first voltage levels applied to at least the first and second control gates are substantially the same and the second and third voltage levels are significantly different from the first voltage levels.

3. The method of claim 1, wherein applying the first voltage levels includes incrementing the first voltage levels through a range of values.

4. The method of claim 1, wherein applying the first voltage levels includes applying pulses of the first voltage levels.

5. In a non-volatile memory including an array of charge storage elements positioned across a substrate surface, a method of coupling voltages to designated ones of the storage elements for simultaneously programming or reading their charge storage states representative of data stored thereby, comprising applying different voltages to a plurality of control gates having lengths extending across the array between charge storage elements that are capacitively coupled with a pair of the plurality of control gates on either side thereof, including placing first voltage levels on those of the plurality of control gates adjacent the designated storage elements and second voltage levels on those of the plurality of control gates not adjacent to the designated storage elements, wherein the first and second voltages are significantly different.

6. The method of claim 5 wherein the first voltage levels placed on those of the plurality of control gates adjacent the designated storage elements are substantially the same.

7. The method of claim 5, wherein placing the first voltage levels includes incrementing the first voltage levels through a range of values in order to read the charge storage states of the designated storage elements.

8. The method of claim 5, wherein placing the first voltage levels includes pulsing the control gates on either side of the designated storage elements with the first voltage levels in order to program the designated storage elements to desired storage states.

9. A non-volatile memory for programming and reading data, comprising:

an array of charge storage elements positioned across a semiconductor substrate,

a plurality of control gate lines extending across the array in a manner that opposing sidewalls of individual charge storage elements are capacitively coupled with at least two of the control gate lines, and

a decoder and voltage supply connected to the control gate lines to couple controlled voltages to the charge storage elements capacitively coupled therewith during programming data thereto and reading data therefrom.

10. The memory of claim 9, wherein the control gate lines are additionally capacitively coupled with the substrate in areas between charge storage elements.

11. The memory of claim 10, additionally comprising trenches formed in the substrate between the charge storage elements in the path of the control lines, the control gate lines extending into said trenches with a dielectric layer between the control lines and the substrate.

12. The memory of claim 9, wherein the memory cells are oriented in a plurality of series connected strings of memory cells, and wherein the control gates extend across multiple strings of memory cells between the charge storage elements.

13. The memory of claim 12, additionally comprising dielectric filled isolation trenches in the substrate between the plurality of strings of memory cells.

14. The memory of claim 12 wherein the control gates include a combination of doped polysilicon as a bottom portion of a height of the control gates and a metal or silicide material in contact therewith as a top portion of the height of the control gates.

15. A non-volatile memory cell array comprising a plurality of strings of series connected memory cells extending in a first direction across a semiconductor substrate, the memory cells including charge storage elements, the array including control lines extending in a second direction across the strings of memory cells and including control gates adjacent charge storage elements thereof, the first and second directions being orthogonal with each other, wherein the control gates are positioned between adjacent storage elements of the memory strings in a manner to be capacitively coupled

with sidewalls of the adjacent storage elements of the memory cell strings on opposite sides of the control gates.

16. The memory cell array of claim 15, wherein the control lines are additionally capacitively coupled with regions of the substrate between the storage elements.

17. The memory cell array of claim 16, wherein the control lines extend into trenches formed in the substrate regions with a layer of dielectric therebetween.

18. The memory cell array of either of claims 11, 16 or 17, wherein the capacitive coupling of the control lines with the substrate regions is characterized by enhancing the conductivity of the substrate regions in response to voltages placed on the control lines.

19. The memory cell array of claim 15, wherein the charge storage elements include conductive floating gates that individually have heights extending above the substrate a distance that is larger than their widths, and wherein the control lines extend above the substrate at least as far as the heights of the floating gates to which the control gates are capacitively coupled.

20. The memory cell array of claim 19, wherein a bottom portion of the control lines includes a doped polysilicon material and a top portion of the control lines includes a metal or silicide material in contact with the doped polysilicon material.

21. The memory cell array of either one of claims 14 or 20, wherein each of said control lines is positioned within the spacing between adjacent ones of the floating gates in order to be electrically isolated from one another.

22. A non-volatile memory system, comprising:

a memory cell array, including:

a plurality of strings of series connected memory cells extending in a first direction across a semiconductor substrate and being spaced apart in a second direction, the first and second directions being perpendicular, the memory cells individually including a charge storage element, and

control gate lines extending in a second direction across multiple strings of memory cells and being positioned in the first direction between adjacent charge storage elements, wherein opposing sidewalls of individual charge storage elements are capacitively coupled with both of the control gates on opposite sides thereof, and

a voltage supply circuit connected to the control gate lines that simultaneously provides (a) first voltages to a pair of control gate lines on opposite sides of at least a first row of storage elements across the plurality of strings in order to raise voltage levels of at least the first row of storage elements to levels sufficient for altering or determining their charge states, and (b) a second voltage different from the first voltage to each of two control gate lines adjacent said pair of control gate lines on opposite sides thereof in the first direction in order to maintain voltage levels of charge storage elements in second and third rows on opposite sides of said at least the first row at levels insufficient for altering or determining their states.

23. The memory system of claim 22, wherein the charge states number in excess of two, thereby enabling more than one bit of data to be stored in each memory cell.

24. The memory system of claim 22, wherein the memory cell array is a NAND array.

25. A method of making a memory cell array on a semiconductor substrate, comprising:

forming a rectangular array of columns and rows of floating gates across a surface area of the substrate with a first layer of dielectric therebetween,

providing isolation of the floating gates across the substrate between columns thereof, and

forming control gates extending across the substrate area perpendicular to said columns between rows of the floating gates in a manner that opposing sidewalls of the floating gates are capacitively coupled with walls of the control gates on opposite sides thereof through a second layer of dielectric and bottom surfaces of the control gates are capacitively coupled with the surface of the substrate over the well through a third layer of dielectric.

26. The method of claim 25, wherein forming the floating gates includes:

depositing a layer of conductive floating gate material over the first layer of dielectric across the surface area of the substrate,

depositing a first type of dielectric material over the floating gate material layer,

removing portions of the first type of dielectric material to leave strips elongated in a direction of the columns and having widths and spaces between them in a direction of the rows according to a minimum resolvable element size,

forming spacers of a second type of dielectric along side walls of the strips of the first type of dielectric material in a manner leaving spaces between the spacers in the direction of the columns that are less than the minimum resolvable element size, and

removing portions of the first type of dielectric material and of the floating gate material layer between the spacers, thereby defining the floating gates with lengths and spaces between them in the direction of the columns that are less than the minimum resolvable element size.

27. The method of claim 26, wherein removing portions of the first type of dielectric material includes forming a mask thereover with widths of strips and spaces therebetween according to the minimum resolvable element size, and thereafter isotropically sideways etching the first type of dielectric material through the mask in a

manner that partially removes the first type of dielectric material under the mask strips, thereby to form the strips of the first type of dielectric material with widths that are less than the minimum resolvable element size.

28. The method of either of claims 25 or 26, additionally comprising, prior to forming control gates, of forming trenches in the substrate surface between the floating gates in the direction of the columns, and wherein forming the control gates includes forming the control gates to extend into said trenches with electrical insulation therebetween.

29. The method of either of claims 25 or 26, wherein forming the control gates includes forming a bottom portion of the control gates from doped polysilicon material and thereafter forming a top portion of the control gates from a metal or silicide material in contact with the doped polysilicon material.

30. The method of claim 29, wherein forming the top portion of the control gates includes forming a continuous layer of said metal or silicide over the array, and thereafter performing a chemical-mechanical-polishing operation to remove an amount of said continuous layer that leaves the top portions of the control gates within the trenches and isolated from each other.

31. A method of forming an array of non-volatile memory cells on a semiconductor substrate, comprising:

forming a layer of conductive material across the substrate with a first layer of dielectric therebetween and a second layer of a first type of dielectric thereover,

removing portions of at least the conductive material and second layer of dielectric in strips having widths in a first direction and having lengths extending across the substrate in a second direction, the first and second directions being perpendicular to each other,

removing portions of the second layer of dielectric through masking elements having dimensions in the second direction according to a minimum resolvable element size in order to form grooves in the second layer of dielectric between masking elements, including removing portions of the second layer of dielectric under the masking elements to reduce the dimensions of remaining islands of the second layer of dielectric in the second direction between opposing sidewalls thereof,

forming spacers of a second type of dielectric along the sidewalls of the islands of the second layer of dielectric with a first set of gaps between the spacers in the second direction,

removing the remaining portions of the second layer of dielectric from between the spacers, thereby forming a second set of gaps between the spacers in the second direction, and

thereafter removing portions of the layer of conductive material exposed in the first and second set of gaps between the spacers, thereby to leave floating gates under the spacers with spaces therebetween in the second direction.

32. The method of claim 31, additionally comprising:

thereafter forming control gate lines having lengths extending in the first direction across the array and being spaced apart in the second direction in the spaces between the floating gates in a manner that sidewalls of the floating gates are capacitively coupled with sidewalls of the control gate lines on both sides thereof through an insulating material therebetween.

33. The method of claim 32, additionally comprising forming [cavities] shallow trenches in the substrate between the floating gates, and wherein forming the control gate lines includes forming the control gate lines extending into [the cavities] said trenches of the substrate with insulating material therebetween.

34. The method of either of claims 32 or 33, wherein forming the control gate lines includes forming bottom portions of the control gate lines to have capacitive

coupling with regions of the substrate between the floating gates through insulating material therebetween.

35. The method of either of claims 32 or 33, wherein forming the control gate lines includes first forming a bottom portion of the control gate lines with doped polysilicon material and thereafter forming a top portion of the control gate lines with a metal or silicide material in contact with the doped polysilicon material.

36. The method of claim 35, wherein forming the top portion of the control gates includes forming a continuous layer of said metal or silicide over the array, and thereafter performing a chemical-mechanical-polishing operation to remove an amount of said continuous layer that leaves the top portions of the control gates within the trenches and isolated from each other.

37. A method of operating a memory array on a semiconductor substrate, wherein strings of a plurality of more than two non-volatile memory transistors are connectable in series to designated bit lines, comprising utilizing potentials on conductive gate elements positioned in capacitive coupling with the substrate in regions between the memory transistors to selectively provide a level of conductivity in the substrate along the strings through such regions.